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Technical Datasheet

takeMS TMS2GB364D08x-138xx

Description

These memory devices are JEDEC standard unbuffered DIMMs, based on CMOS DDR3 SDRAM technology using DDR3 SDRAMs in FBGA packages on a 240-pin glass epoxy substrate. The memory array is designed with Double Data Rate (DDR3) Synchronous DRAMs for unbuffered applications.

Fly-by command/address/control bus architecture of DDR3 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth. This main benefit of DDR3 is made possible by its 8 bit prefetch buffer.
DDR3 memory ensures a power consumption reduction of 30% compared to DDR2 modules due to DDR3's 1.5 V supply voltage, also defined as "Enhanced low power features".

These modules feature Serial Presence Detect (SPD) based on a serial EEPROM device. DDR3 SPD programming is based on a speed bin. DDR3 latencies are numerically higher because the clock cycles by which they are measured are shorter. Absolute latency (ns) is generally equal to or faster than DDR2.

Features
240-pin Unbuffered DDR3 SDRAM
JEDEC standard 1.5V I/O
Fly-by command/address/control bus with on-DIMM termination
On-die I/O calibration engine
On-Die Termination (ODT)
Serial Presence Detect (SPD) with EEPROM
High precision calibration resistors
Impedance controlled 6-layer PCB Technology
JEDEC standard form factor (133.35 mm x 30.0 mm)
READ and WRITE calibration
Improved thermal design
Operating Temperature 0°C ~ 75°C

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Technical details

- **2048 MB longdimm module**
- **128Mx8 IC organisation**
- **x64 module organisation**
- **1333MHz / PC3 10600**
- **double sided / 16 ICs**
- **CAS Latency 8 at max. memclock**

For pin configuration please check www.takems.com/support/index.php
If you have any questions regarding our products you can contact us via email: info@takems.com

Order-No.: **TMS2GB364D08x-138xx**

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